Generalized Fractional-Order Complex Logistic Map and Fractals on FPGA

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Abstract. This paper introduces a generalized fractional-order complex logistic map and the FPGA realization of a corresponding fractal generation application. The chaotic properties of the proposed map are studied through the bifurcation behavior and maximum Lyapunov exponent (MLE). A concise fractal generation process is presented, which results in designing and implementing an optimized hardware architecture. An efficient FPGA implementation of the fractal behavior is validated experimentally on Artix-7 FPGA board. An example of fractal implementation is verified, yielding frequency of 24.34 MHz and throughput of 0.292 Gbit/s. Compared to recent related works, the proposed implementation demonstrates its efficient hardware utilization and suitability for potential applications.

Introduction

Chaos is mentioned in systems that are sensitive to initial conditions such that a small variation cause a significant difference in behavior. Chaotic systems are distinguished by their attractive characteristics like randomness, aperiodicity and fractal identity. Fractals are recognized by their complex geometric structures such as the ones generated from Mandelbrot and Julia maps [1]. Chaotic systems are classified into continuous-time maps and discrete-time maps. The discrete maps are classified into integer-order maps that can be extended to fractional such as logistic and tent maps, and real maps that can be extended to complex such as logistic and Gaussian maps. Several works introduced fractal generation from integer-order complex discrete maps including logistic and Gaussian maps [2, 3, 4]. Realizations in digital hardware have become more practical for industrial use. Fixed-point operations are widely used for hardware realizations to save costs and enhance speed. The generalization of conventional chaotic systems into the fractional-order domain allows more accurate understanding of the map behavior, increases the degree of freedom in design and enhances its performance in applications. Fractional-order discrete chaotic maps are employed in several applications such as encryption, neural networks, synchronization and multi-scroll generation. Among several fractional definitions, EL Raheem definition is simple and suitable for hardware implementation [5]. This paper proposes a generalized fractional-order complex logistic map, fractals and their FPGA realization. The chaotic properties of the proposed map are studied using bifurcation and MLE diagrams. The proposed hardware implementation of the fractals based on the fractional-order complex logistic map utilizes simplified steps. The fractal behaviors are validated experimentally on an Artix-7 FPGA kit. The proposed implementation is compared to recent related works demonstrating its hardware efficiency and suitability for potential applications.

Results and discussion

The proposed design for fractals based on the generalized fractional complex logistic map is written in Verilog HDL with the simulation of Xilinx ISE 14.7 and implemented on Xilinx FPGA Artix-7 XC7A100TCSG324 by using Chip scope. The outputs are wired to a 12-bit Digital to Analog converter, which is connected to a digital oscilloscope to display the fractal behavior. The fractal example is realized and validated experimentally on FPGA. The design achieves frequency of 24.34 MHz and throughput of 0.292 Gbit/s. A summary of FPGA implementation results of this work and other implemented fractal works [2, 3, 4] is presented. The proposed implementation consumes higher resources and lower frequency than [3, 4] due to the excessive arithmetic operations needed for the fractional domain. On the other hand, the proposed implementation achieves efficient hardware utilization and speed than [2] due to the simplicity of operations of the proposed map than Gaussian map. The proposed realization is considered a promising solution to increase the degrees of freedom in the design and enhance the performance in different applications such as encryption schemes and multi-scroll generators.

References

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